TM-104-12-83

TECHNICAL MANUAL

DISTRIBUTOR'S MANUAL

OMEGA-TEK

MODELS MK____

OMNIBOARD

This manual supersedes TM/104, 4ARIL1981

OMEGA-TEK SHELBY, OHIO 44875

BOX 185

4 APRIL 1984

INDEX

APPENDIX

NOTICE

WARRANTY

All OMEGA-TEK P.C. Boards are guaranteed to be free of defects in materials and workmanship for 5 years from date of delivery. Any board found defective during the warranty period will be repaired or replaced at the discretion of OMEGA-TEK. Warrantee shall pay the shipping charges to and from OMEGA-TEK for in warranty repairs.

Boards damaged from physical or electrical abuse or improper soldering techniques are excluded from the warranty. OMEGA-TEK shall be the sole judge as regards the definition of physical or electrical abuse or improper solder technique.

Rev 12-6-85

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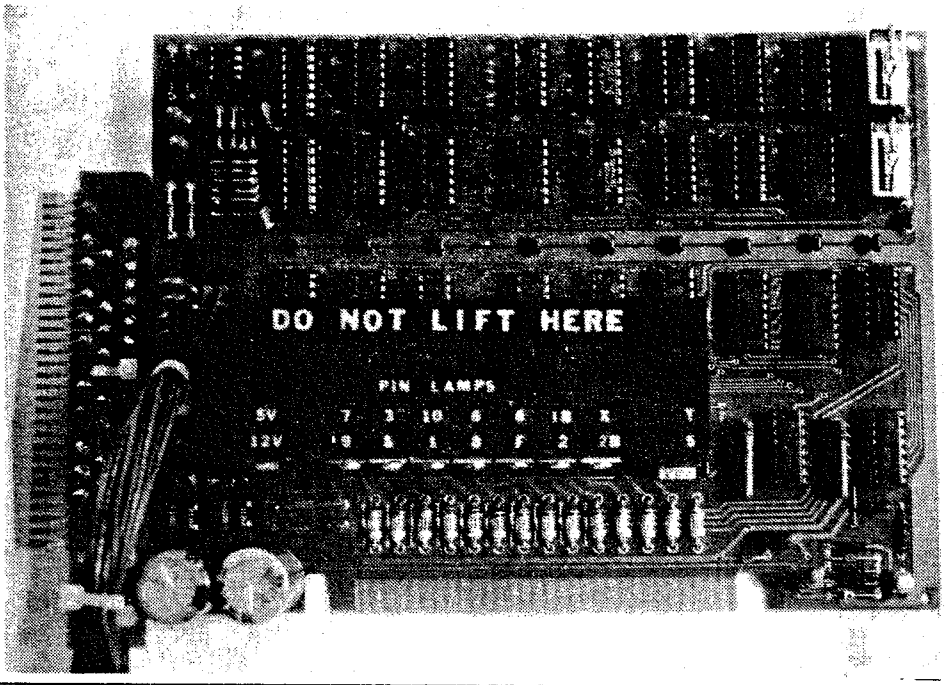
TECHNICAL BULLETIN: OMEGA-TEK P.C.BOARD MODEL MK-1,2

TB/100 Rev. 4-6-81



DESCRIPTION: The OMEGA-TEK **MK-1 P.C.Board** is designed as a direct replacement for the following components of the 82-70 Solid State Chassis: PC-1, PC-2, PC-3, PC-4, PC-5, & Auxiliary Board.

The following components inside the chassis box are automatically bypassed when the MK-1 Board is installed: Pin Lamp Triac, Capacitors CP-1 (10V), CP-2 (pin lamp filter), CP-3 (150v), Diodes D-2, D14 through D23, KX Relay and PC connectors 1,2,3,&6.

Absolutely no wiring changes are required and all pinspotter functions remain identical to those of origional boards.*

A full 18 month warranty is provided (see order contract).

Additionally, the MK-1 P.C.Board is designed to be customer serviceable with a voltmeter and/or logic probe.

Operating Specifications:

Line voltage at Pinspotter	90-125 Volts AC • 50/60 HZ
Ambient operating temperature range	35° F-125° F
Board power consumption at pinspotter zero	2 watts

Each board is thoroughly tested and run in a powered up state for 100 hours at 110° F and retested prior to shipment.

* The MK-1 is not compatible with the 82-140 or 82-225 Sparemaker.

II. INSTALLATION: OMEGA-TEK OMNI BOARD

The following procedures should be followed to facilitate installation:

1. Disconnect the Russell-Stoll plug (i.e. 110v) at Pinspotter.

CAUTION

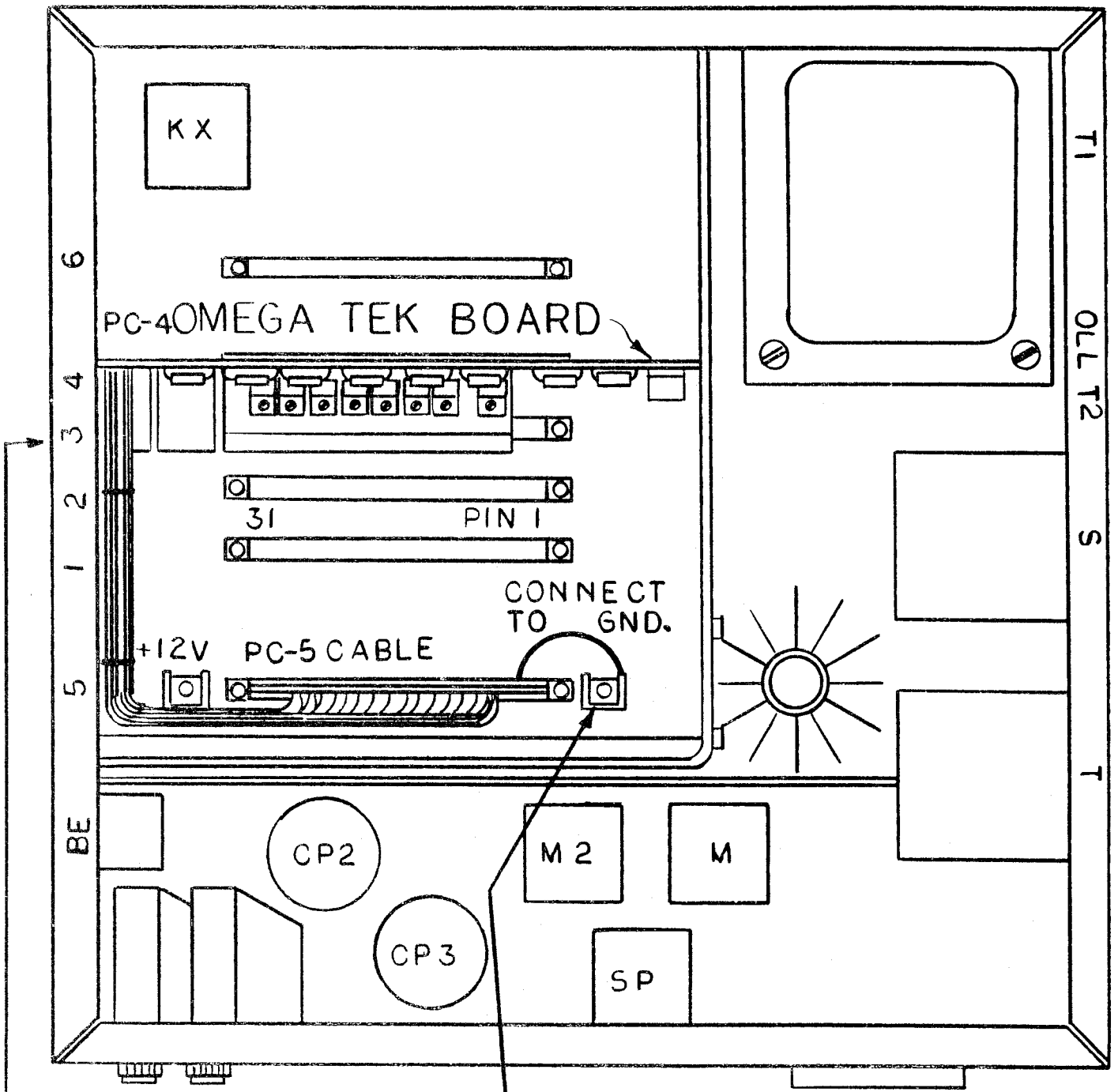
REMOVAL OF THE 3 CONDUCTOR "RUSSELL-STOLL" CONNECTOR PLUG IS THE ONLY ACCEPTABLE METHOD OF DISCONNECTING 110V POWER FROM THE PINSPOTTER DURING INSTALLATION OF THE OMNI BOARD. ANY OTHER METHOD OF REMOVING POWER FROM THE PINSPOTTER IS NOT ACCEPTABLE, AND COULD RESULT IN SIGNIFICANT SHOCK HAZARD.

2. Remove P.C. boards 1,2,3,4, and 5. The Auxiliary Board may be removed or left in place as desired.
3. Carefully inspect the PC4 and PC5 receptacles for bent or broken pins and for cracked or broken housings. On the PC3 receptacle only pins 10 and 11, 13, and 20 need be serviceable.
4. Locate the 3 lug ground tab connector directly adjacent PC5 (see Fig.1 on reverse side) and insure that at least 1 lug is free of connections. If all lugs are full, install the chair terminal provided to allow 2 of the EXISTING wires to occupy the same terminal so as to leave 1 terminal free. Do not confuse the GROUND lugs with the identical 12v lugs at the opposite end of the PC5 receptacle.
5. Install the loose piece jumper plug provided into the PC3 receptacle.
6. Install the MK-2 board in the PC4 receptacle. Install the attached cable connector into the PC5 receptacle.
7. Connect the green GROUND lug provided for in step 4.
8. Plug in the Russell-Stoll plug.

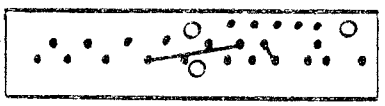
Installation is now complete. Pinspotter functions should now be identical to those of the old boards.

CAUTION

WAIT AT LEAST ONE MINUTE AFTER TURNING OFF POWER BEFORE INSERTING OR REMOVING THE OMNI BOARD FROM THE CHASSIS.



GROUND IF CHAIR TERMINAL NECESSARY, USE FRONT LUG ONLY FOR CHAIR.



LOOSE PIECE ADAPTER. INSTALL IN PC 3 RECEPTACLE WITH GOLD FINGERS TOWARD PC 4.

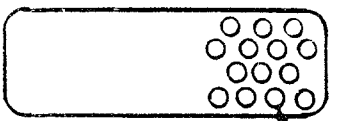


FIG. 1

OMEGA-TEK	
SHELBY, OHIO	
	DRG: 104

TM/104 REV. 4-25-81

CAUTION

THE GREEN GROUND WIRE MUST BE ATTACHED

TO THE GROUND LUG AS SPECIFIED IN STEPS 4 AND 7

OR DAMAGE TO THE P.C. BOARD WILL RESULT.

III. Transistor Theory and Testing

In the majority of industrial and digital applications, the transistor is simply used as an on-off switch. Fig. 2 shows a relay operated lamp circuit and its transistorized equivalent.

Instead of applying the control signal across the coil to light the lamp as in the case of the relay, we now use a transistor and apply a control signal of proper polarity between emitter (common) and base. If this signal is sufficiently positive in polarity with respect to common, the transistor will abruptly turn "on" and electrons will flow from emitter to collector and through the lamp.

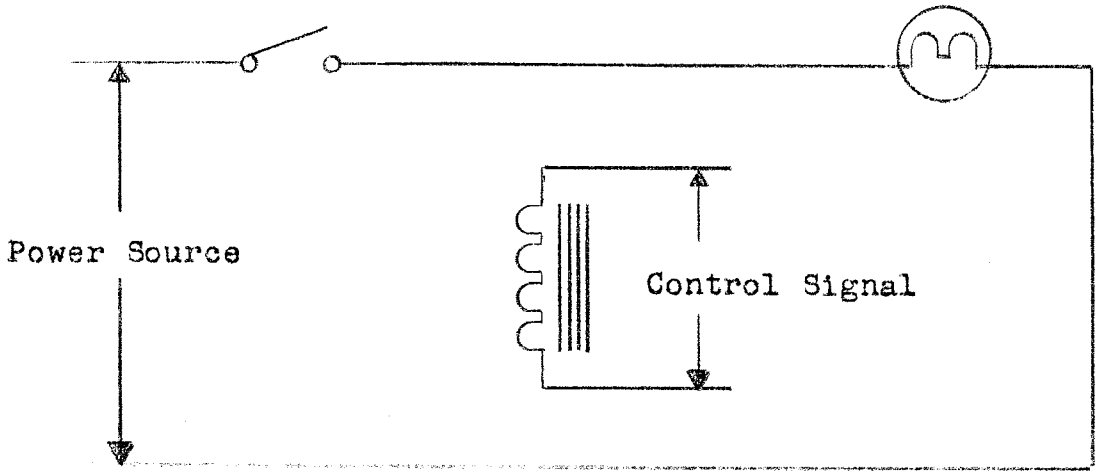
If the control signal is of sufficient amplitude, the transistor will be fully "saturated" and collector current will rise to a point limited only by the impedance of the external load (i.e. the lamp).

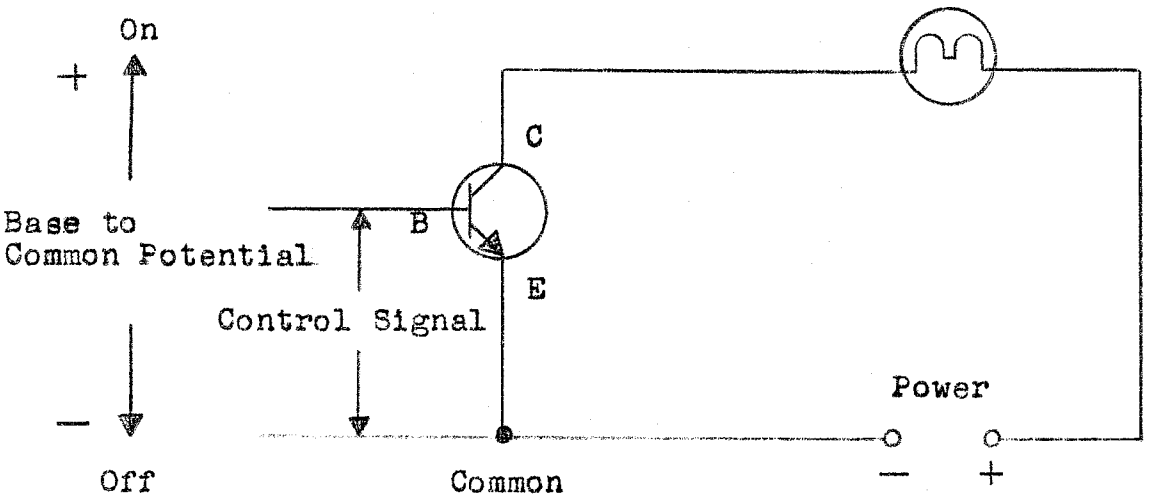
Conversely, lowering the amplitude of the control signal to a small amplitude with respect to common or going negative with respect to common will cause the collector current to decrease and eventually approach zero. In this condition, the transistor may be said to be in its "off" state.

Fig. 2 shows a transistor device designated as an NPN transistor. There is a second common bi-polar device known as the PNP which differs somewhat in characteristics from the NPN. It is shown in Fig. 2. Note the difference between the symbol for NPN and PNP. If the PNP were used in the same circuit as Fig. 2 the result would be the circuit shown in Fig. 3.

It will be noted that the power source connections have been reversed. This is due to the difference in internal physics between the two types.

In addition, it will now be noted that the control signal must become increasingly negative with respect to common to achieve saturation "on".


Power Source
Control Signal


On
+
Base to
Common Potential
C
B
E
Control Signal
—
Off
Common
Power
—
+

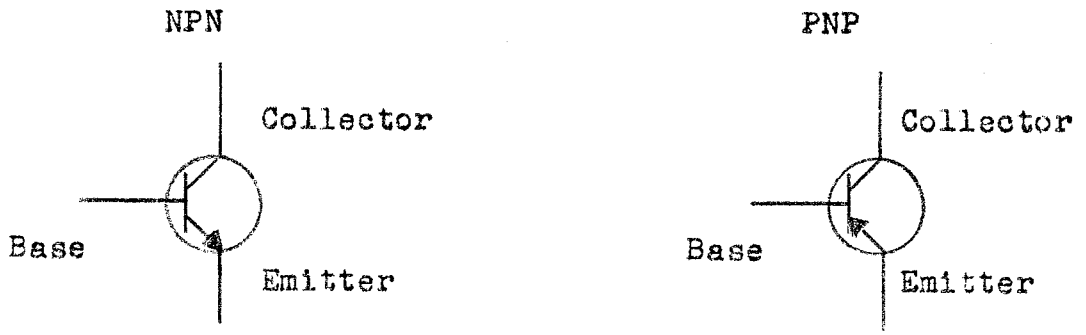

NPN
Collector
Base
Emitter
PNP
Collector
Base
Emitter

FIG. 2

PNP Equivalent of Fig. 2

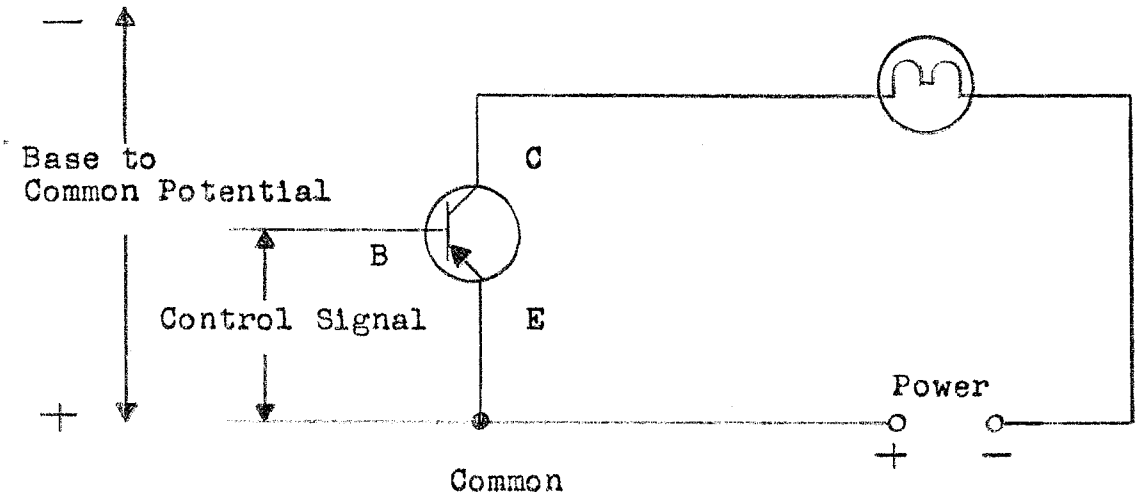


FIG. 3

Conversely, the signal voltage must become nearer the common potential or even positive with respect to common to achieve turn off. Except for these major differences, the two types, NPN and PNP, correspond rather closely in all other details. We will be dealing with both types.

At this point, there are a few rules of thumb in dealing with both types of transistors which must be memorized before proceeding to more complex circuits. These are:

1) Any potential (signal) applied between base and emitter (common) of a polarity such that the potential of the base rises toward the potential present at the collector will at some point cause the transistor to turn on.

2) Conversely, any potential applied between base and emitter of a polarity such that base is brought nearer the emitter potential (common) will at some point cause the transistor to turn off.

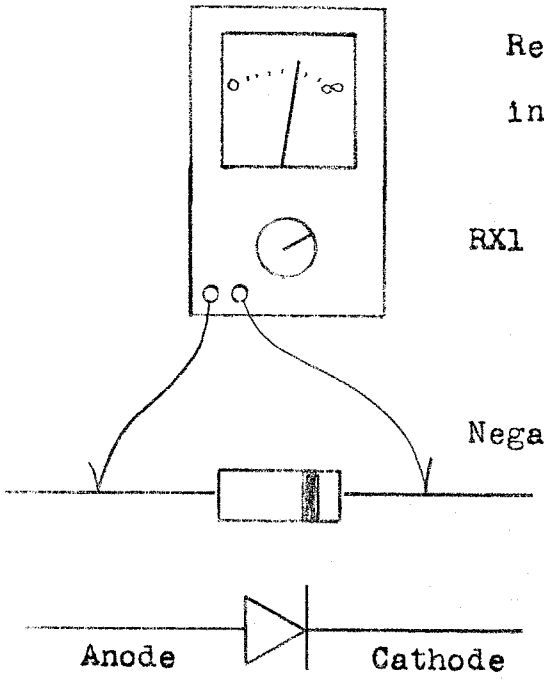
As an example, looking at Fig. 1 we see the positive pole of the power source connected to the collector. Therefore, any signal at the base which approaches this positive potential will tend to turn the transistor on.

Before proceeding further, there are a number of simple tests which can be performed on transistors and diodes that will give some indications useful to the technician.

Using the ohmmeter on the RX1 scale, it is possible to test diodes and transistors in circuit for shorts and opens. Keep in mind this test is not 100% valid and depends largely on relatively high ohmic values of components shunting the device under test in order to get useable results.

The test method for a diode is shown in Fig. 4. Keep in mind the positive and negative leads of a voltmeter may or may not be the positive and

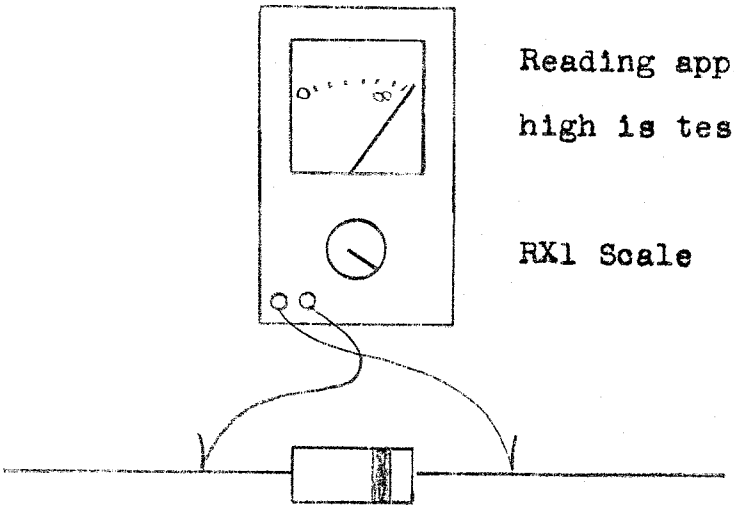
Step 1



Reading approx. mid-scale both in-circuit and out.

RX1 Scale

Step 2



Reading approx. infinite or very high is tested in-circuit.

RX1 Scale

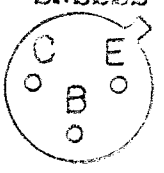
FIG. 4

2N3905

Bottom View

FIG. 5

2N2222



negative leads when using the meter for ohms measurement. If this proves to be the case Steps 1 and 2 will be reversed.

This test is capable of telling us two things with relative certainty and a crude indication of a third item. These are:

1) With diode forward biased (schematically electrons flow from negative to positive and against the arrow in diodes and transistors) as in Step 1, we know the diode junction is intact if we read approximately mid-scale on RX1. This tells us:

   A) The junction is not open.

   B) The junction is not shorted.

If we read infinity or zero, on the other hand, we would know the junction was open or shorted respectively.

Reverse biasing the diode as in Step 2 gives a crude indication of reverse leakage. If a reading is obtained on RX1, disconnect one lead of the diode and repeat. If reading is still present, diode is defective. If reading goes to the infinity, diode probably is OK. Switch to RX10K and repeat. A reading very close to infinity should be obtained.

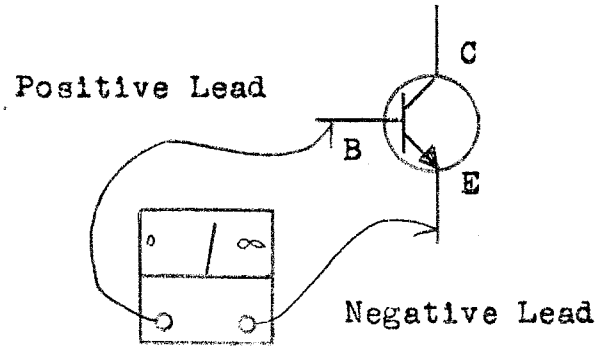
Transistors may be checked in a similar manner. To do this, it is necessary to identify emitter, base and collector.

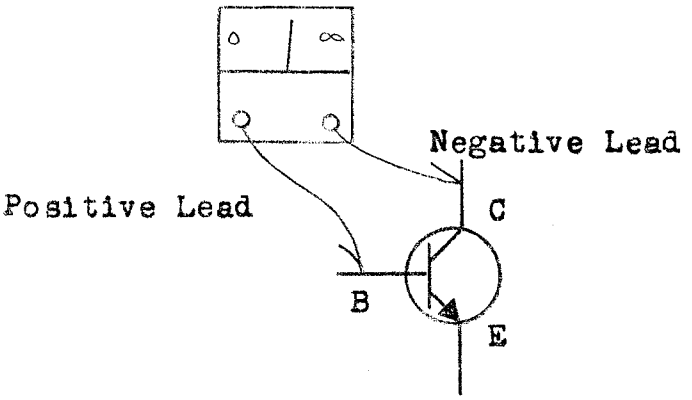
A transistor manual will be necessary to identify any transistor not listed in Fig. 5. Having done this, proceed as in Steps 1 and 2 in Fig. 5A.

No attempt will be made to reverse bias these junctions in circuit as shunt resistance is usually too low for accuracy. Steps 1 and 2 can be performed in circuit.

Again as with the diode, this test can detect a shorted or open junction. These conditions comprise the majority of transistor failures.

NPN Transistor Test

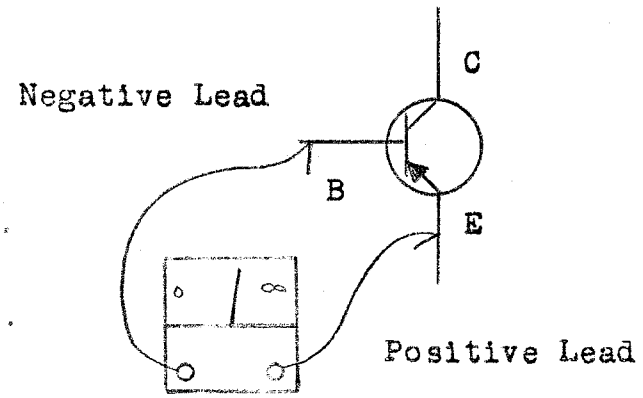


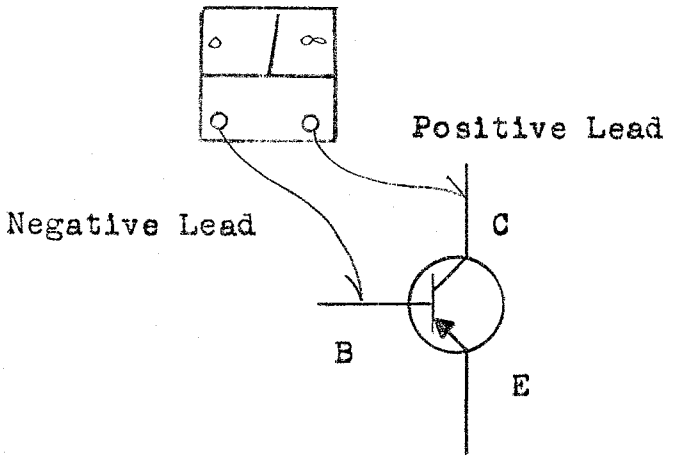


Meter on RX1 Scale.

Reading approx. mid-scale.

PNP Transistor Test





Meter on RX1 Scale.

Reading Approx. mid-scale.

FIG. 5A

IV Logic Gates

The following section details the various logic gates that comprise the circuitry of the OMEGA-TEK board.

A detailed explanation of gate logic theory can be obtained from any elementary electronic textbook and will not be presented in detail here. We will, however, present truth tables for aid in understanding the various gate functions.

All integrated circuit logic gates, except one, are of CMOS construction. CMOS presents the following advantages over standard TTL logic:

1) CMOS power dissipation is quite low. Typical static power dissipation is 10 nano-watts per gate. Even at 1 MHZ with a 50pf load power dissipation is still less than 10 milli-watts.

2) Noise immunity approaches 50%, typically being 40% of the full logic swing.

For testing purposes, valid logic levels are as follows:

Logic 0	1.5 volts or less
Undefined	1.5 to 3.5 volts
Logic 1	3.5 volts or more

These levels must be measured with either a high impedance FET voltmeter to avoid loading or with a logic probe set for CMOS logic levels.

Pin connections are shown on the schematic and drawings of each chip are shown on the pages of the parts list in section VIII.

Some explanation should be offered of the 74C76 JK flip-flop and of the 74C174 D flip-flop.

A flip-flop is essentially a circuit which can remember data that may no longer may be present at the input.

Data will be retained until power is removed or, in some cases, until clear inputs are activated or data again changes in some specified manner.

The 74C76 has two JK type flip-flops. Outputs Q and $\overline{Q}$ will change states on the falling edge of input data pulses, provided the preset and clear are at the correct levels. The J and K inputs can be used to further control the actions of the flip-flop as shown in the truth table. These inputs are used to recreate the data present at outputs Q and $\overline{Q}$ prior to a power down. We use this flip-flop and associated circuits to remember what cycle the pinspotter is in and whether or not the time delay has elapsed. This information is retained during a power down and is reloaded into the flip-flop during a power up.

The 74C174 has six D type flip-flops. Data present on the D inputs is transferred to the Q outputs and latched there on the positive edge of a pulse at the clock input.

The data is constant at the Q outputs until the D inputs change and the flip-flop is again clocked.

Clear will force all Q outputs low at any time.

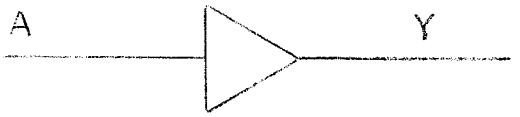
This flip-flop remembers pins standing.

Finally, something should be said about the 14490 digital de-bouncers used on the input circuits. These chips are used to eliminate any switch bounce or noise that may be present at the various inputs to the board.

These chips have a self contained clock and $4\frac{1}{2}$ bit register.

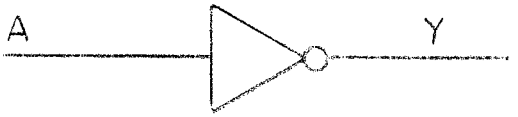
The chip is capable of integrating both up and down and can be used to de-bounce both openings and closures. There is no fixed delay input as with some RC arrangements. The output simply does not shift until four clock pulses after the input has stabilized.

14050 HEX BUFFER



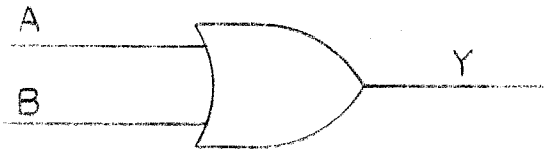
A	Y
H	H
L	L

74C04 — 71C14 HEX INVERTER



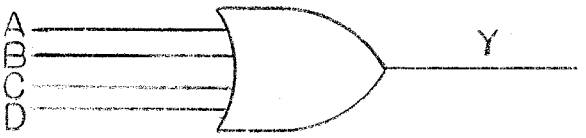
A	Y
H	L
L	H

74C32 2-INPUT OR



A	B	Y
H	H	H
H	L	H
L	H	H
L	L	L

14072B 4-INPUT OR

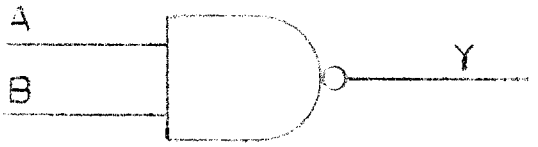


A	B	C	D	Y
L	L	L	L	L
ANY OTHER SET OF INPUTS				H

74C08 2-INPUT AND

A	B	Y
H	H	H
H	L	L
L	H	L
L	L	L

74C00 2-INPUT NAND



A	B	Y
H	H	L
H	L	H
L	H	H
L	L	H

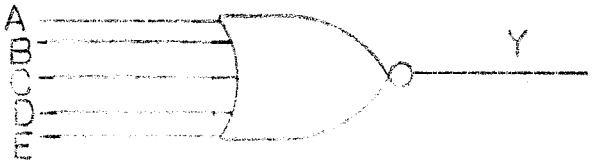
74C02 2-INPUT NOR

A	B	Y
H	H	L
H	L	L
L	H	L
L	L	H

14025B 3-INPUT NOR

A	B	C	Y
H	L	L	L
L	H	L	L
H	H	L	L
L	L	H	L
H	L	H	L
L	H	H	L
H	H	H	L
L	L	L	H

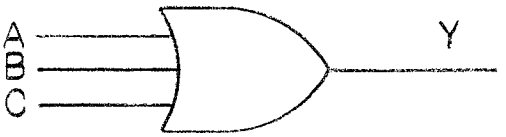
74LS260 5-INPUT NOR



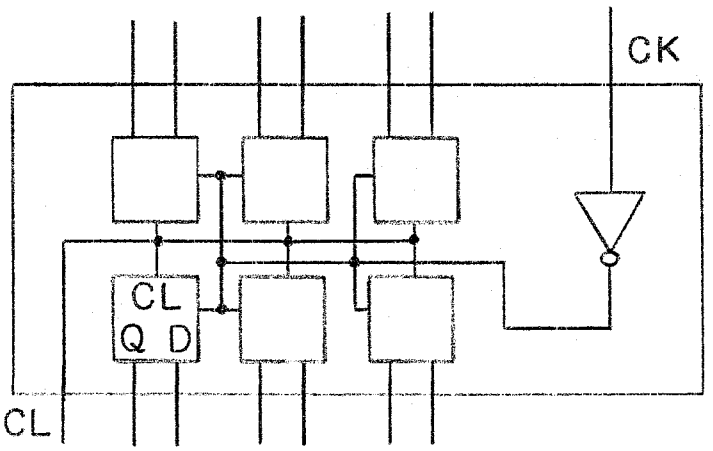
A	B	C	D	E	Y
L	L	L	L	L	H
					L

ANY OTHER SET OF INPUTS

14075B 3-INPUT OR

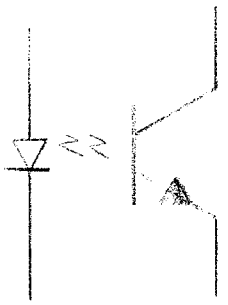


A	B	C	Y
H	H	H	H
H	H	L	H
H	L	H	H
H	L	L	H
L	H	H	H
L	H	L	H
L	L	H	H
L	L	L	L

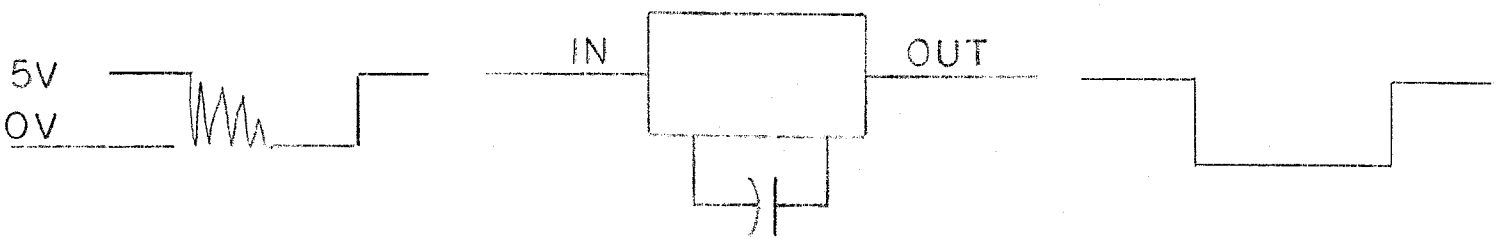


74C174 HEX D FLIP-FLOP

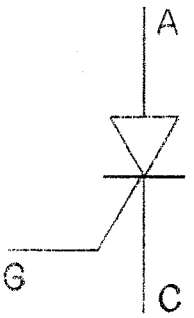
ILQ-74 ILD-74



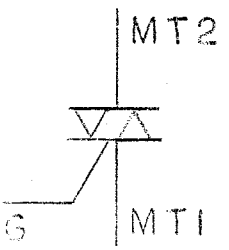
14490



S2010LS2



2N6071



The operation of the SCR's and TRIAC's can be obtained from any textbook. As used here, they are simply power switches for lamp and relay control.

We are now ready to see how the previously discussed gates are used to form the elementary circuits of the OMEGA-TEK board.

V Board Logic Circuits

The power down circuit is shown in Fig. 6. With power turned on approximately 35 volts appear at the cathode of the zener with respect to ground. Since the zener is a 24 volt device, it will conduct producing a voltage drop across R1. C1 will begin charging through R2 and the voltage at the R2, R3, C1 junction will after a time t_2 become high enough to turn Q1 on. the input of the Schmitt inverter will then be at logic low and the output will go high.

When voltage is removed, the zener will stop conducting as the voltage falls below 24 volts. C1 will begin to discharge quickly through diode D1 and the relatively low value of R1. Q1 will, after a short time t_1 turn off, causing the input of the inverter to go high and the output low. This condition will last until the power supply has fallen to below 3 volts, at which time, the IC's will cease to function.

It is necessary to have this circuit to insure that data is stored in the memory from the flip-flops in an orderly fashion during power down and that during power up, data in memory is properly transferred and loaded into the flip-flops and that the latches come up in the proper state.

A slight delay is provided at power up to allow the voltages at the IC's to stabilize before releasing data. The delay is bypassed during power down to allow the data to be stored in memory at the earliest sign of a power loss.

The R-S Latch

An R-S latch of the type used on the OMEGA-TEK board is shown in Fig. 7. It is essentially a flip-flop composed of logic gates and operates in the following manner: When power is applied, the Q and $\overline{Q}$ outputs may come up in either state. By holding reset low during power up we can always insure that Q comes up low and that $\overline{Q}$ comes up high. Set input is normally high during this time. Once the flip-flop has been reset, the reset line goes high and the latch is ready to be triggered. A low pulse to the set input will now cause Q and $\overline{Q}$ to invert. The outputs will remain inverted until reset or until power is removed.

The latch is used to remember the occurrence of an off spot, strike, or foul.

Ball Memory

The ball memory circuit is shown in Fig. 8. With power on and stabilized, the last set of conditions shown in the truth table are met and the flip-flop will change output states (toggle) on the falling edge of any pulse into pin 6. As output states change, the appropriate coil of a latching reed relay is energized. Since the PWR line is high, either coil is free to energize when the corresponding output is high. Also, the contacts at pins 1 and 7 have no effect when PWR is high. As PWR goes low, pins 1 and 6 of U9 go low halting any further changes of memory. Also, either pin 8 or pin 7 of the flip-flop will be pulled low depending on which relay contacts are closed. This will insure that the flip-flop will not change states as the power goes down. Similarly, as power comes up, the PWR line is held low until voltages stabilize insuring that the flip-flop is either cleared or preset exactly as

it was when power went down. When PWR goes high the flip-flop is ready to respond to the falling edge of input pulses.

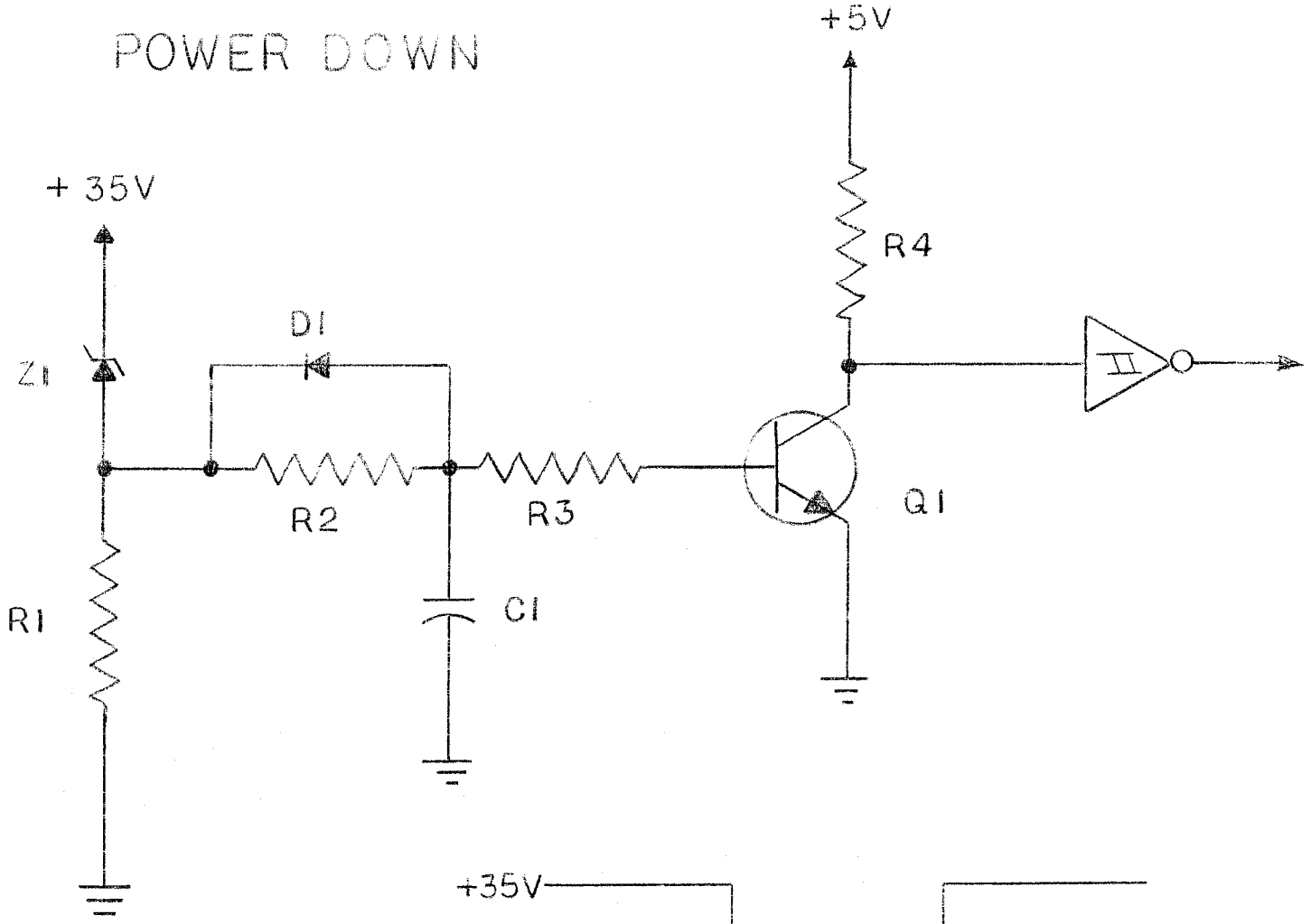
The ball memory remembers whether the machine is in first or second ball.

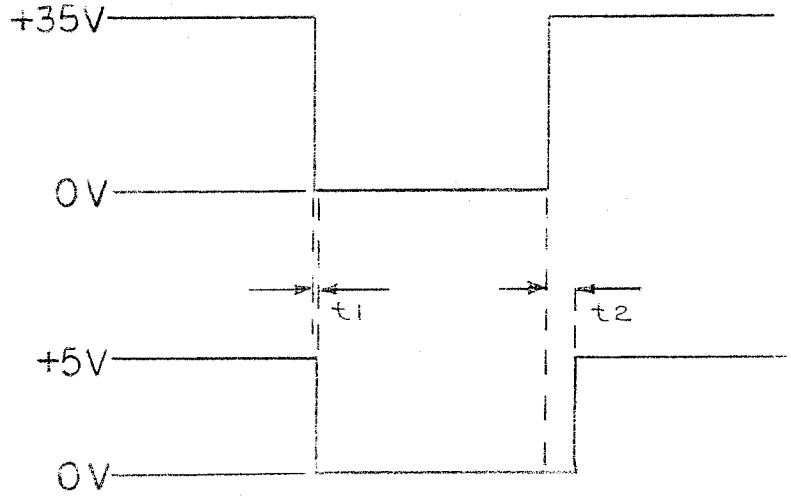
Time Delay Memory

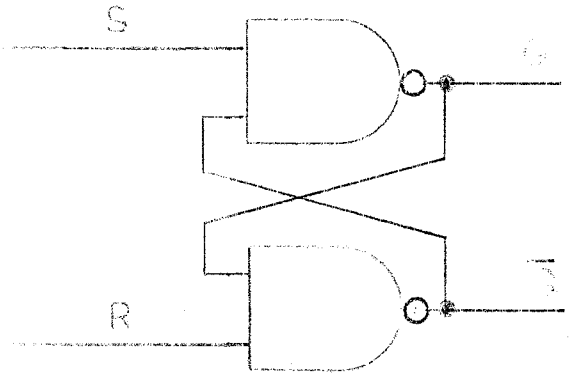
The final circuit to be discussed is the time delay memory in Fig. 9. The time delay memory works in the same fashion as the ball memory except that input K is held low all the time. This means the output state will change only once on the falling edge of the first input pulse. Further, input pulses will produce no change in output states. A pulse at TDRS activates the clear input to return the flip-flop to its original state. Memory is retained during power down and power up in the same fashion as the ball memory.

The time delay memory remembers whether or not the three second time delay has elapsed in the machine cycle.

POWER DOWN



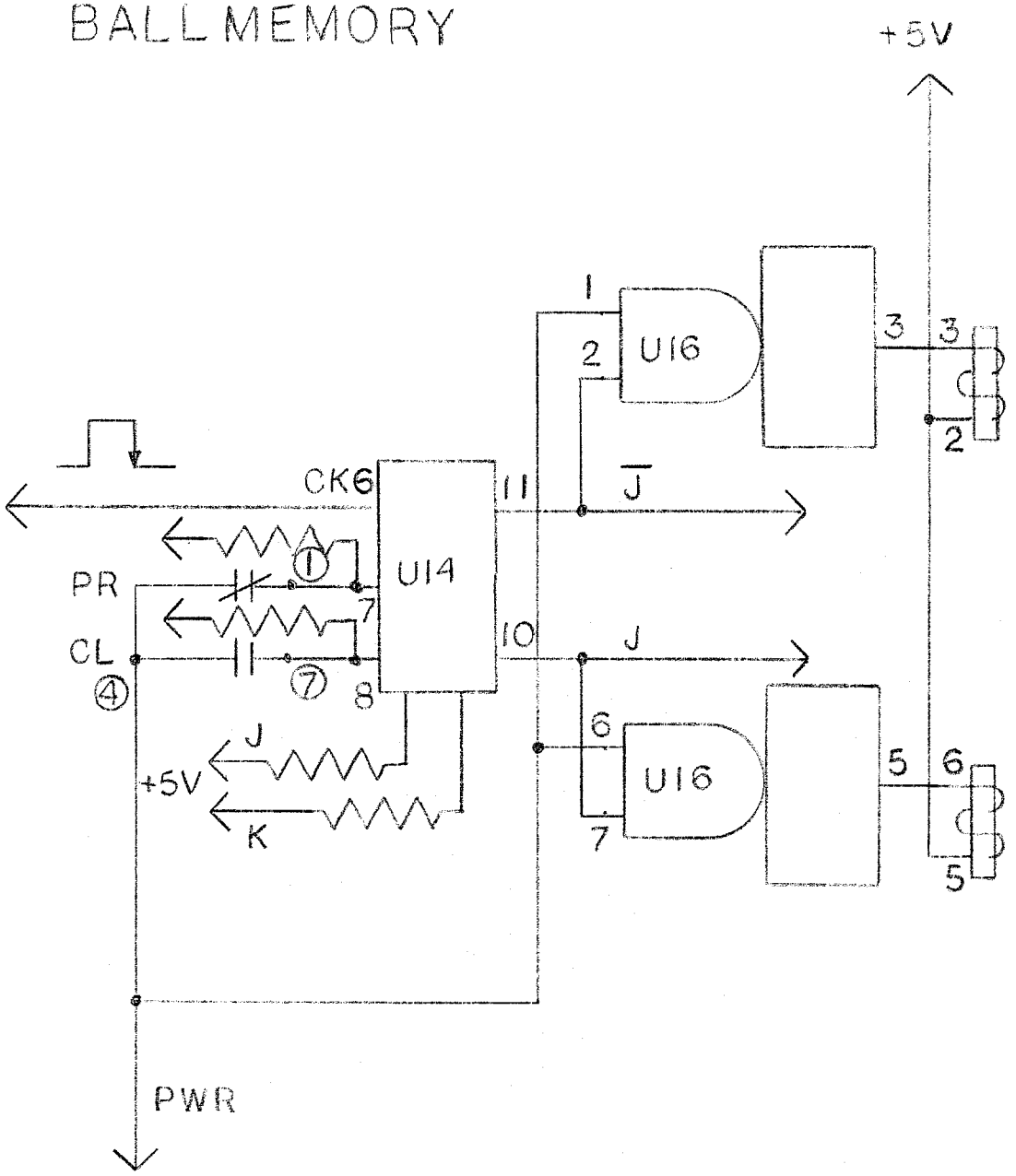




R-S LATCH

FIG. 7

BALL MEMORY

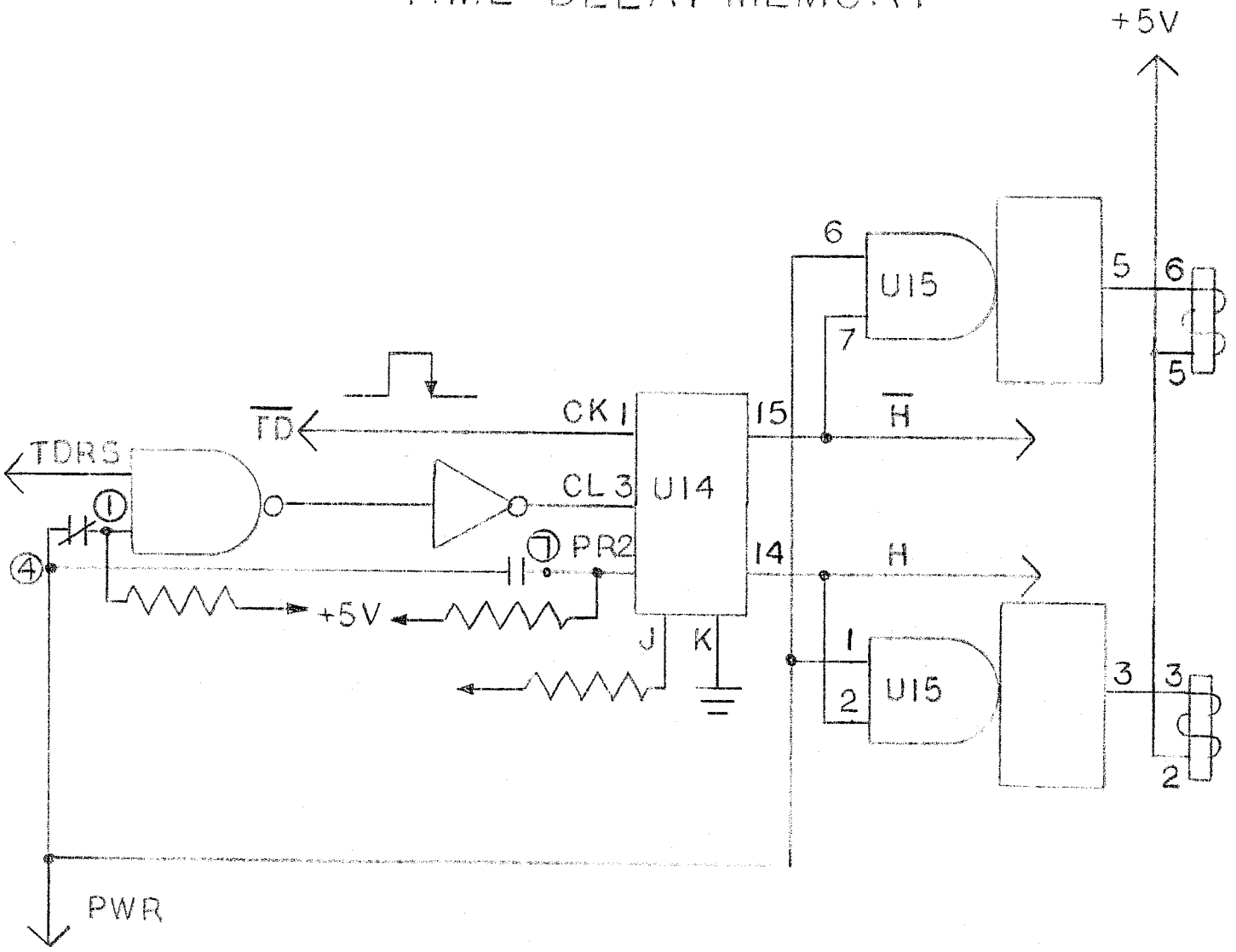


INPUTS					OUTPUTS	
PR	CL	CK	J	K	Q11	Q10
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\overline{Q0}$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

COIL 2-3 CONTACTS 1-4
COIL 5-6 CONTACTS 4-7

FIG. 5

TIME DELAY MEMORY



INPUTS					OUTPUTS	
PR	CL	CK	J	K	Q15	$\overline{Q}$14
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\overline{Q}$0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

COIL 2-3 CONTACTS1
COIL 5-6 CONTACTS4

FIG. 3

VI Theory of Board Operation

Definitions: Reference is made to schematic 0018 (MK-1 and MK-2) in Appendix A. Logic states are indicated by letters signifying various inputs and outputs. Logic states shown as A, B, OS etc. are at logic 1. Logic states shown as $\overline{A}$, $\overline{B}$, $\overline{OS}$ etc. are at logic zero.

The schematic shows the machine at zero with power on, in 1st. ball and with bin switch open.

First Ball Cycle

Power up: When power is first applied and exceeds 24V at Z1, Q1 is held off by the charging time of C3, R3. U2-13 input is high and U2-12 output is low. This low output insures that the strike, foul, and OS latches are reset. Additionally, U3-2 is held high to insure that the machine doesn't cycle during power up. Data is retained in memory by keeping U8-1, 6 and U9-1, 6 inputs low. The flip-flops in U7 are cleared or preset at this time depending on the state of relays K1 and K2.

When C3 is fully charged, Q1 will turn on, U2-13 will go low and U2-12 high. This now allows all latches and flip-flops to become active.

Sweep runs to 66°: When the start switch closes momentarily, output U10-6 E goes low. U3-1 goes low, U3-3 goes low, U20-8 goes low causing U20-9 to go low. This causes U19-10 and U19-8 to go low, latching a start into U3-2. U14-8 goes low, U14-10 goes high causing U20-5 and U20-6 to go high turning on Q3 and starting the sweep run to 66°.

Sweep at 66°: When the sweep reaches 66° B & $\overline{B}$ invert. U20-2 goes high, U19 unlatches, U14-8 is high, U14-10 is low causing U20-5 and U20-6 to go low turning off Q3. Also, if the gripper protection switch is closed, all inputs

at U20-11,12,13 will now be low. This will cause Q2 to turn off allowing C4 to charge through R7 and after 3 seconds the time delay flip-flop U7 H & $\overline{H}$ will invert.

U15-9,10,11,12 will now be low. U15-13 will be high, U19-1 and U19-3 will be high turning on Q5 and starting the table.

Table runs to 260°: At 260° the grippers will detect standing pins. If all pins are standing, all gripper inputs at U27 and U28 will be low. U27 and U28 outputs will be high. All inputs to U26 will be high. This logic 1 present at at least on U16 input is sufficient to block a low at U17 which would cause a strike cycle.

Also, at 260° C & $\overline{C}$ invert. U6-9,10,11,12 are now low, U6-13 high, U22-10 low and U24-9 and U25-9 low.

As sweep restarts (via U6-2,3,4,5 low, U6-1 high, U4-1 low, U23-3 low, U5-5 low, U5-6 high and U5-9 high, H already inverted, and Q3 on) and passes 86° $\overline{L}$ inverts, U6-13 goes low, U22-10 high. On the rising edge of this pulse to U24-9 and U25-9 pin data is transferred to the Q outputs, causing the pin lamp SCR's to turn on. This data will be present on U24 and U25 outputs until reset.

The sweep will continue to run until SA closes at 270°. This causes A & $\overline{A}$ to invert. U5-9 will go low causing the sweep to stop at 270°. As sweep passes 186°, B & $\overline{B}$ are restored to original states. Output $\overline{L}$ also restores. The table continues to run through TA-1 185-355°, and U15 and U19. At 185° of second table revolution TA-1 U1-13 will go low causing the time delay to be reset via TDRS. H & $\overline{H}$ restore.

As the sweep runs up from 270° and the table passes 260° the concurrent overlap of SA and TA-2 will generate a pulse into the ball cycle memory U7-6

and will switch the ball memory to 2nd ball on the falling edge of the pulse. J & $\overline{J}$ invert.

The overlap of SA and TA-2 is an extremely critical adjustment. It is necessary to explain this condition in detail in order to understand why this is so.

Assume that the pinspotter has 12 RPM motors. This means that 1 rev. takes 5 sec. Since a complete revolution is 360°, this means that 1° of revolution of either the table or sweep requires .0138 sec.

Assume the machine is on 1st ball with the sweep at 270° and the table commencing its 2nd revolution. At 270° A & $\overline{A}$ invert this acts as an enable for for the two NOR gates connecting to U7-6. As the table passes 185° of its second revolution the sweep is activated and starts its run back to zero. At 260° of the table run C & $\overline{C}$ invert causing the input to U7-6 to go high. If either the sweep A or the table C now goes low this will cause the ball memory to shift. Usually the sweep will reach zero first causing the machine to go to second ball.

As above if the sweep starts to run up when the table passes 185° and the required overlap condition is not present until the table reaches 260° then this means the sweep has run 75° of its total run of 90° to get back to zero before the table TA-2 reaches the required state. This leaves 15° of overlap to generate the high pulse required to insure changing to 2nd ball. This is an overlap of 2/10ths of a second. This is sufficient for a properly adjusted machine but for machines with worn switches and questionable adjustment it may be necessary to adjust or replace TA-2 to insure proper operation with the OMEGA-TEK board as well as with the original boards.

Second Ball Cycle

Initial conditions are identical to 1st ball except J & $\overline{J}$ are inverted. Cycle start, sweep stop at 66°, and time delay are discussed in 1st ball cycle. At 66° B & $\overline{B}$ invert. U6-2,3,4,5 are low U6-1 high, U4-1 low and U23-3,11 low causing U24 and U25 to reset, turning off the pin lamps.

After time delay H & $\overline{H}$ invert U5-3 is now high causing U5-6 to be low. U5-9 is now high causing Q3 to turn on and sweep to run.

At 270° A & $\overline{A}$ will invert causing U5-9 to go low turning off Q3 and stopping sweep.

When the bin switch closes U15-2,3,4,5 will be low causing U15-1 to go high. This will cause U18 to pull in spot relay and turn on Q5 causing table to run.

As table passes 185° TA-1 will close causing TDRS to reset the time delay U-7.

Table continues to run through TA-1 (185-355).

Since inputs at U5-11,12,13 are now low, U5-10 will be high and sweep will run from 270-360° until A & $\overline{A}$ revert.

As the table passes 260° C & $\overline{C}$ are inverted. U14-2,3 inputs are now low causing U14-1 to go high. As both table and sweep approach zero both C & $\overline{C}$ and A & $\overline{A}$ revert, the latter causing U14-4 to go high. This causes 14-1 to go low and J & $\overline{J}$ revert causing U7 to reaturn to 1st. ball.

Strike Cycle

All conditions are the same as first ball cycle except no pins standing.

When the sweep reaches 66° after 3 seconds H & $\overline{H}$ will invert. U15-9,10, 11,12 are now low. U15-13 is high causing U19-3 to be high. Q5 turns on and the table runs.

Since no pins are standing, inputs to U27 and U28 will be high. U27 and U28 outputs will be low. U26 output is high and U4-10 low causing strike memory to set. Output from the strike memory turns on the strike light and holds off the second ball light. U14-6 is at logic high and U14-4 low. U15 has the strike input high to hold the table at 360° for spotting.

Also, as the table passed 260° C & $\overline{C}$ inverted causing a pulse at U7-6. This caused the first ball light to go off (2nd ball is held off by the strike memory).

At this point, inputs to U6 $\overline{L}$ & $\overline{B}$ are low. C is high causing U6-1 to be low. U4-1 is then high. U23-3 is also high. U5-6 goes low causing U5-9 to go high and U20-6 high turning on Q3 and causing the sweep to run through to 270°. At 270° A & $\overline{A}$ invert causing the sweep to stop.

Spotting and sweep action is now as discussed in 2nd ball cycle.

The strike memory is reset when H & A revert to original states as table and sweep approach zero.

Foul Cycle

The foul signal is optically coupled to the input via U29 into U1. U1 output will cause the foul lamp to come on for the length of the foul signal.

The foul memory will not set until the sweep has reached 66°.

After the 3 second time delay, the foul memory output will hold U15-9 high preventing table run. U5-4 is high causing U5-6 to remain low. When the time delay inverted U5-1,2,8 are now low and U5-9 high, causing U20-6 to be high and Q3 to turn on. The sweep will then run until A & $\overline{A}$ invert at 270° stopping the sweep. U14-11 is high and U14-13 is low. When the bin switch closes, all inputs at U15-2,3,4,5 will be low and the table will spot pins and run.

Further table and sweep action is as discussed in 2nd ball cycle. Foul memory is reset when J & $\overline{J}$ revert at the end of the cycle.

VII

MAINTENANCE AND TROUBLESHOOTING GUIDE

ALWAYS HANDLE THE MK-2 BOARD CAREFULLY:

° Avoid flexing circuit board during installation and handling.

° Avoid flexing wiring on connector plug during handling and installation.

° Avoid touching the foil pattern on the circuit board during handling and installation.

° Always store P.C. boards in shipping container when not in use.

° Always use P.C. board puller when removing P.C. board.

° Always remove Russell-Stoll connector before installing or removing P.C. board.

° Always wait one minute to allow 150v DC to discharge after removal of Russell-Stoll plug before inserting or removing MK-2 board.

° Always insure that cover is on chassis and that chassis is latched to pinspotter after installation.

WHEN TROUBLE SHOOTING ALWAYS BE SURE THAT:

° MK-2 board and attached PC-5 connector are fully seated, and that there are no broken connectors or bent pins on PC-4, PC-5 and PC-3 receptacles.

° Besure that PC-3 jumper board is correctly installed and seated. Chassis will not spot pins and mask switch will not cancel pinlamps if jumper is improperly installed.

° Be sure green ground wire is connected to terminal lug at PC-5.

THE CUSTOMER IS AUTHORIZED TO PERFORM THE FOLLOWING PROCEDURES AND TESTS SHOULD DIFFICULTIES BE ENCOUNTERED:

° Insure the PC4 & PC5 receptacles are in good order and that the green GROUND wire on the PC5 connector cable is securely connected to the GROUND lug adjacent PC5.

° Check for continuity from this lug to the chassis frame with an ohmmeter.

° Insure that C2A-12F (fig.1) terminal is not damaged and that there is continuity from C2A-12F to the chassis frame.

° Insure that the GROUND wire at the Russell-Stoll plug is in place and that there is continuity from the ground pin to the machine frame.

° Insure the incoming power has a satisfactory EARTH GROUND by means of an outlet tester or visual inspection.

° Insure the screw securing the 2 lug terminal strip to EARTH GROUND IS TIGHTENED SECURELY. (Remove bottom cover and locate strip under CP-3 and inspect)

° Should the pinspotter fail to change from 1st ball to 2nd ball during a cycle or during 10th frame use, inspect and replace SA and/or TA-2 switches as required to insure proper operation. (Refer to pinspotter service manual for locations) OMEGA-TEK will replace any MICRO-SWITCH that fails to operate with the MK-2 board.*

IF DIFFICULTIES PERSIST, THE FOLLOWING PROCEDURE SHOULD BE FOLLOWED:

1. Determine by substitution whether board or chassis is at fault.
2. If board is at fault, carefully describe the nature of the problem and return to OMEGA-TEK for warranty repair. Use only the yellow warranty card provided.

*Start switch and mechanically broken switches not included.

Digital troubleshooting techniques are covered in the text furnished with the spare parts kit and will not be covered in this manual aside from information already presented.

Some general observations are offered to anyone attempting to repair the Omniboard.

1. The problem must be isolated to a particular part. Random replacement of components rarely fixes the problem and quite often results in damage to the board.

2. The most difficult part of the repair job, one the problem is isolated, is replacement of the defective component, in particular, IC's.

3. There are several techniques for removing IC's from P.C. Boards. We have found the following to be the most effective:

Using the diagonal cutters supplied, snip the legs of the IC off at the point where they enter the plastic package.

Using the soldering iron supplied, heat each pin in turn from the solder side of the board while, simultaneously, gripping and pulling the pin with needle nose pliers from the component side of the board.

When all pins have been removed in this fashion clear the holes of solder with the vacuum bulb provided in the spare parts kit.

REMEMBER

The vacuum bulb must be cleared of solder after EVERY instance of useage. A wire gauge is provided for this purpose.

If the hole is not completely cleared of solder after two tries with the vacuum bulb, more solder must be flowed into the hole and the process started over again.

WARNING

Most damage to P.C. Boards occurs in trying to get out that last little bit of solder still blocking the hole. To little solder allows excessive heat build up on the foil itself with subsequent damage.

In attempting to remove capacitors and SCR's in the TO-220 package it is best to attempt to heat all leads simultaneously. In the case of the capacitors this is easily done by using the broad tip supplied with the soldering iron. In the case the TO-220 packages with three leads, it is best to heat two adjacent leads and tilt the package so as to work these out of the board and then to heat the remaining adjacent leads.

WARNING

Insure adequate solder is present on the connection and use the least amount of heat possible when attempting this.

REMEMBER

Always use the flux remover to clean repaired solder joints as this allows visual inspection of the actual solder coating on the component lead.

P.C. Boards obtained from surplus houses are the best tool for learning to remove components without damaging the P.C. Board. Consult one of the many hobbyists magazines to locate the nearest dealer in surplus and scrap P.C. Boards. It is well worth the time and modest cost involved.

VIII. Parts List

The following list may be used to identify the parts on the board. Reference should be made to schematic 0018 in Appendix A.

U1	14409VP
U2	74C14
U3	74C08
U4	74C02
U5	14025
U6	14002
U7	74C76
U8	DS3632N
U9	DS3632N
U10	14490VP
U11	74C08
U12	74C04
U13	74C00
U14	74C02
U15	14002
U16	14072
U17	74C00
U18	DS3632N
U19	74C32
U20	14075
U21	14075
U22	74C02
U23	74C08
U24	74C174
U25	74C174
U26	74LS260
U27	14049
U28	14049
U29	ILD-74
BR1	VM-18
BR2	VM-18
VR1	MC7805CT
VR2	MC7812CT
TR1	2N6071A
TR2	2N6071A
SCR1-14	S2010LS2
MOV1-7	39ZA1
FZ3-16	GFA 10amp
Q1	2N2222
Q2	2N3906
Q3	2N2222
Q5	2N2222

CR1-10	1N914	MK-1	1N4004	MK-2
CR11-17	1N4004			
CR18-28	1N914			
Z1	1N5252			
C1	4.7 uf 35v			
C2	4.7 uf 35v			
C3	4.7 uf 35v			
C4	22 uf 16v	Tantalum		
C5	.1 uf 50v			
C6	.1 uf 50v			
C7	.1 uf 50v			
C8	1000 uf 50v			
C9	.47 uf 50v			
C10	.1 uf 50v			
C11	1000 uf 50v			
C12	.47 uf 50v			
C13				
C14				
C15	1000 pf 50v			
C16	1000 pf 50v			
	.1 uf 50v	all bypass capacitors		
R1	1k ¼w			
R2	1K ¼w			
R3	10K ¼w			
R4	10K ¼w			
R5	1K ¼w			
R6	10K ¼w			
R7	120K ¼w			
R8	100 ¼w			
R9	220 ¼w			
R10				
R11	100 ¼w			
R12	220 ¼w			
R13				
R14	10K ¼w	MK-2		
R15	10K ¼w	MK-2		
R16				
R17	33 3w			
R18	75 3w			
MK-2	P.C. 5 Connector			
U1-5	ILD-74			
D1-10	1N4004			
R1-10	3.3K ½w			
C1-3	.1 uf 50v			
C4	.47 uf 50v			